

HIGH-SPEED CLOCK DIVISION

FIELD OF THE INVENTION

The present invention relates generally to high-speed clock division, and particularly to apparatus and methods for multi-stage division of high-frequency clock signals.

BACKGROUND OF THE INVENTION

In many different applications, handling of high-speed clock signals is necessary, such as but not limited to, data communication, wherein receivers may recover a clock signal from incoming data. For example, the clock signal may subsequently be used to sample the incoming data in order to generate a new data signal, which has been re-timed or synchronized with the recovered clock signal.

If the clock is a high-speed (i.e., high frequency, the terms being used interchangeably throughout) clock, dividing its frequency by a specific number in order to count bits of the data may comprise complicated and large circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood and appreciated more fully from the following detailed description taken in conjunction with the appended drawing, which is a schematic illustration of a method and circuit for high speed clock division in accordance with an embodiment of the invention.

5

09976298-101501

DETAILED DESCRIPTION OF THE PRESENT INVENTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present invention.

Some portions of the detailed description that follows are presented in terms of algorithms and symbolic representations of operations on data bits or binary digital signals within a computer memory. These algorithmic descriptions and representations may be the techniques used by those skilled in the data processing arts to convey the substance of their work to others skilled in the art.

An algorithm is here, and generally, considered to be a self-consistent sequence of acts or operations leading to a desired result. These include physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers or the like. It should be understood, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities.

Unless specifically stated otherwise, as apparent from the following discussions, it is appreciated that throughout the specification discussions utilizing terms such as "processing," "computing," "calculating," "determining," or the like, refer to the action and/or processes of a computer or computing system, or similar electronic computing device, that manipulate and/or transform data represented as physical, such as electronic, quantities within the computing system's registers and/or memories into other data similarly represented as physical quantities within the computing system's memories, registers or other such information storage, transmission or display devices.

Embodiments of the present invention may include apparatus for performing the operations herein. This apparatus may be specially constructed for the desired purposes, or it may comprise a general purpose computer selectively activated or reconfigured by a computer program stored in the computer. Such a computer program may be stored in a

computer readable storage medium, such as, but is not limited to, any type of disk including floppy disks, optical disks, magnetic-optical disks, read-only memories (ROMs), compact disc read-only memories (CD-ROMs), random access memories (RAMs), electrically programmable read-only memories (EPROMs), electrically erasable and programmable read only memories (EEPROMs), magnetic or optical cards, or any other type of media suitable for storing electronic instructions, and capable of being coupled to a computer system bus.

Reference is now made to the single drawing, which illustrates a method and circuit for high speed, dual modulus clock division in accordance with an embodiment of the invention. A high-speed clock signal *Clock in* may enter a dual-modulus counter, comprising without limitation a pass gate 10 and a frequency divider (or divider-by-two) 12. Frequency divider 12 may comprise, for example, a D-type (i.e., delay type) flip-flop (D-FF) that feeds its Q-bar output into its data input. Such a divider may be easily constructed for high clock speeds.

The output of frequency divider 12 may be fed to a multi-bit counter 14, also referred to as a multi-bit divider 14. In the illustration, multi-bit counter 14 may comprise a 6-bit counter to which data inputs DIN<1:7> may be input, and which outputs a clock out signal (clkout or *Clock out*). However, it is emphasized that the invention is not limited to these values, and the invention may be carried out with 4-bit, 8-bit and any other amount of bits. In general, multi-bit counter 14 may comprise a 2^n -bit counter to which data inputs DIN<1:(2^n-1)> may be input. Multi-bit counter 14 may further divide the clock frequency, which has already been divided by frequency divider 12, in accordance with the data inputs DIN. In other words, the counter 14 may count clock cycles and Clock Out may be asserted once in a certain number of the clock cycles, said number being specified by the data inputs.

The control of the count (i.e., division) precision of multi-bit counter 14 may comprise controlling bit 0 of the DIN input with control logic circuitry. Multi-bit counter 14 may be controlled by its DIN 1:7 inputs. The dual-modulus counter may be controlled by bit 0, which may make the dual-modulus counter count to 3 instead of 2 on the first "small" cycle of a "large" division cycle. The control logic circuitry may comprise without limitation one or more flip-flops, such as a divider control flip-flop (FF) 16 and a count control FF 18. As seen in the illustrated embodiment, the logic circuitry may comprise

without limitation the following connections and inputs: The count control FF 18 may have three inputs: *clk*in from *Clock in*, FF set from a reset signal (*rst*), and data from the *clk*out output of multi-bit counter 14. The count control FF 18 may output to an inverter 20. A gate 22 may AND the output of inverter 22 and the *clk*out output of multi-bit counter 14. Gate 22 may output to an inverter 24, whose output in turn may be input as data to the divider control FF 16. The divider control FF 16 may have two other inputs: *clk*in from *Clock in*, and FF set from reset signal *rst*. A gate 26 may AND the output of divider control FF 16 and the *DIN*<0> bit. The output of gate 26 may be fed to pass gate 10 and an inverter 28 connected to pass gate 10. Frequency divider 12 may receive input from *clk*in and *rst*. Multi-bit counter 14 may receive input from *clk*in, *DIN*<1:(2ⁿ-1)> and *rst*. It is noted that the multi-bit *clk*in input may be fed by the *clk*out output of the frequency divider 12.

Division of a high-frequency clock signal (*Clock in*) may be accomplished in two or more stages. For example, in a first stage, the clock signal may be divided in two by frequency divider 12. Alternatively, the clock signal may be divided by a different number. For example, as described hereinbelow, the pass gate 10 may be controlled by the control logic circuitry to divide the signal by three (3). As mentioned above, the clock signal may be further divided by multi-bit counter 14 in accordance with the number specified by the *DIN* inputs. The output is the divided clock signal *Clock out*.

In one embodiment, the divider control FF 16 and the count control FF 18 may sample at the *Clock in* frequency, which may be a very high frequency. When the multi-bit counter 14 outputs a "1", e.g., once in a count cycle, the control logic circuitry may close the pass gate 10 for one *Clock in* cycle, if the *DIN*<0> bit is set, meaning that a count value required is odd. If the required count value of the *DIN* is even, no action may be taken. After this cycle, the pass gate 10 may open again, and remain open until the next count of the multi-bit counter 14. Thus, the pass-gate 10, when closed, allows a delay of one clock cycle, and may enable the first counting stage to divide the signal in three instead of two. In this manner, the second stage's count (whose input is the divided clock) may also get delayed by one cycle, thereby performing the division by an odd value, and enabling full programmability over the whole data <0:6> bit range. The delay by one clock cycle may enable using a simple initial stage divider, while maintaining full programmability of the counter.

It is appreciated that larger counters may be used to divide the signal into other divisions, such as but not limited to 5 or 6, for example. A $2/3$ divider may be significantly smaller and easier to construct, however, than other dividers, such as a $5/6$ divider. In many applications, a frequency division of two may be sufficient to construct a counter with adequate count precision for a high number of bits. The only elements that may have to function at the high speed of *Clock in* are the divider control FF 16, the count control FF 18 and the rest of the control logic circuitry.

It will be appreciated by persons skilled in the art that the present invention is not limited by what has been particularly shown and described herein above. Rather the scope of the invention is defined by the claims that follow: